

Appl No. 10/084,543**PATENT**
IBM Docket No. FR920010006US1**Amendments to the Abstract:**

Replace the Abstract with the following new Abstract paragraph:

A method and a logic are disclosed for performing Cyclic Redundancy Check (CRC) calculation N-bit at a time which accelerates checking in the binary string data packet d-bit wide Field Check Sequence (FCS). The CRC codes are d-bit wide binary vectors of a multiplicative cyclic group generated by a polynomial generator of degree d ($G(X)$). An N-bit chunk of the binary string is divided, modulo $G(X)$, to obtain a d-bit wide division result while a current value of the d-bit wide FCS is displaced N in the multiplicative cyclic group. Then, the d-bit wide division result and the displaced d-bit wide FCS are added to become the new current FCS. The above steps are repeated until no data bits are left, thus getting the final result of the CRC calculation which can be used either for checking or for generating the FCS.